

APS Storage Ring Monopulse RF BPM Upgrade*

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Abstract. The Advanced Photon Source (APS) is a third-generation synchrotron light source in its ninth year of operation. The storage ring monopulse radio frequency (rf) beam position monitor (BPM) was designed to measure single-turn and multi-turn beam positions for operations and machine physics studies. Many of the components used in the original design are obsolete and costly to replace. In this paper we present a proposal to upgrade the monopulse rf BPMs in which the existing system hardware is repartitioned and the aging data acquisition system is replaced. By replacing only the data acquisition system, we will demonstrate a cost-effective approach to improved beam stability, reliability, and enhanced postmortem capabilities. An eight-channel ADC/digitizer VXI board with sampling rate of up to 105 MHz (per channel) and 14-bit resolution coupled with a field-programmable gate array and embedded central processing will provide the flexibility to revitalize this system for another decade of operation. We will discuss the upgrade system specifications, design, and prototype test results.

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INTRODUCTION

The Advanced Photon Source (APS) is a third-generation synchrotron x-ray source that provides intense x-rays for basic and applied research. The stability of the beam is largely dependent on the resolution and accuracy of the beam position monitor (BPM) system. The APS storage ring presently makes use of 280 monopulse radio frequency (rf) BPMs designed to measure single-turn and multi-turn beam positions. The rf BPM signal processing topology is a monopulse amplitude to phase (AM/PM) technique for measuring the beam position in the x- or y-axis [1]. A logarithmic amplifier channel measures the beam intensity. The processing electronics are located above the tunnel in 40 VXI crates with up to 9 BPMs per crate. The rf BPM system front-end and timing system was upgraded in 2001 [2,3], but the overall system performance has suffered because of an aging data acquisition system. The rf BPM data acquisition is presently being handled in a VXI-based signal conditioning and digitizing unit (SCDU) [4]. Each SCDU module provides signal conditioning for beam position in the x or y plane and sum signals. The sum signal is peak detected and the normalized position data is integrated on the SCDU. Both signals are digitized via 12-bit ADCs and stored in output registers. These registers are read at 271 kHz (revolution frequency) for up to nine BPMs by the memory scanner module in the same VXI crate via the local bus. Each VXI crate has a memory scanner and beam history module. The memory scanner

provides a programmable (2-2048 turn) boxcar averager for each BPM x and y position. It also provides a high-speed fiber-optic port to stream data to the feedback system.

There are many programmable logic device chips on this module that have grown obsolete and are therefore very expensive to support; additionally there are only a limited number of spare boards available after nine years of operation.

The data from the VXI local bus are also shared with the beam history module. This module provides storage memories for each BPM for postmortem analysis. The 32-k by 32-bit memory operates as a first-in first-out (FIFO) buffer and is capable of storing approximately 50 milliseconds of storage ring BPM data. This module suffers from many of the same problems realized in the memory scanner.

RF BPM UPGRADE PROPOSAL

The upgrade approach repartitions the existing system hardware such that the rf section from the button electrodes to the receiver output remains electrically the same and the data acquisition system is replaced as illustrated in the shaded areas in Fig. 1. This approach removes the monopulse receiver from the VXI-based SCUDU and locates it in a designated EMI-shielded chassis. This has many mechanical advantages such as improved cooling and ease of replacement. The receiver's center frequency remains at 352 MHz with an intermediate frequency bandwidth of 10 MHz. The receiver interface card shown in Fig. 1 will provide the control interface for self-test, gain selection, commutation, and horizontal or vertical plane measurement selection.

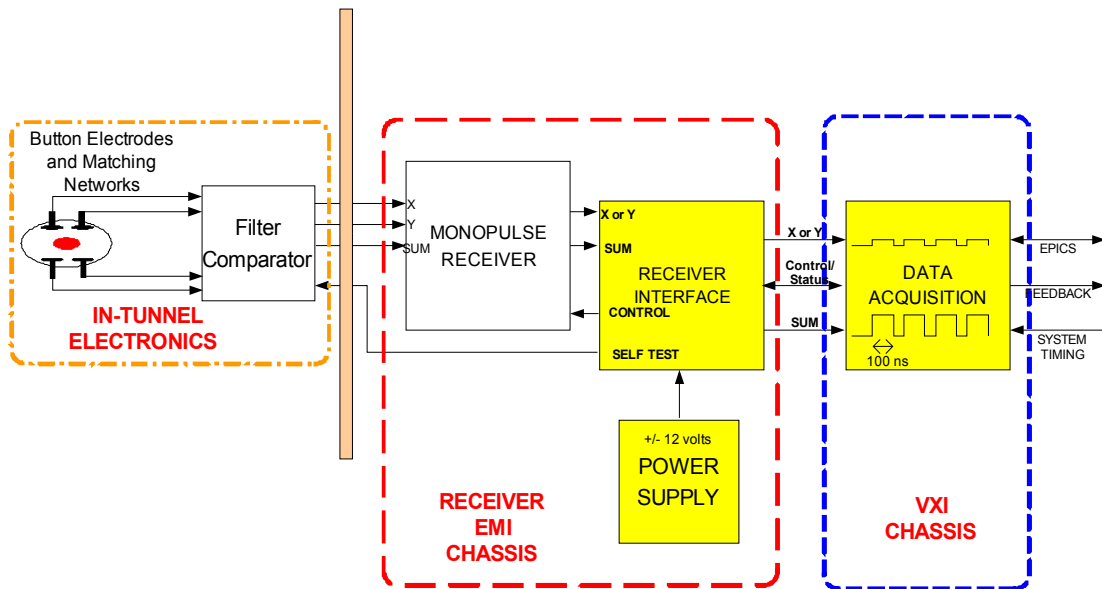


FIGURE 1. System block diagram.

DATA ACQUISITION DESIGN

The proposed data acquisition block diagram shown in Fig. 2 is an eight-channel ADC/digitizer VXI board. A single VXI board will provide the data acquisition for up to four BPMs. The gated integrator and peak detectors used in the SCDU data processing are replaced by ADCs running at a beam-synchronized frequency of 88 MHz (one quarter of the rf frequency). Presently the SCDU data acquisition only acquires data for a single 50-ns sample per turn regardless of the fill pattern. The proposed upgrade system can measure a single bunch per turn or all of the bunches in the train in a 10-MHz bandwidth. This allows for more measurements per turn, resulting in a reduction of the noise floor scaling as \sqrt{N} , where N is the number of samples collected. The present trend at the APS points toward increasing the number of buckets being filled. If we assume a typical fill of 24 or 324 bunches with six coherent samples per bunch, a resolution improvement of a factor of 12-18, respectively, can be implied.

The design will have many reconfigurable functions. We are presently evaluating the Lattice ispPAC[™] 80 [5] for the ADC input lowpass filter shown in Fig. 2. In-system programming allows reconfigurable gain and cutoff frequency. We are presently working on trade-off studies to determine the filter requirements to minimize bunch-pattern dependence.

This upgrade also facilitates a new feature or mode of operation called “oscilloscope,” which will stream data in a 10-MHz bandwidth. This will be useful in machine studies to analyze bunch-to-bunch instabilities as higher currents are explored.

ADC Front End

At the time of selection we found two data converters that met our initial criteria of having greater than 12 bits and the ability to sample at an integral divisor of our rf frequency (351.929 MHz) for easy synchronization. The two converters we found were the Analog Devices AD6645-105 [6] and the Texas Instruments ADS5500 [7]. The Analog Devices converter was chosen for several reasons including having better published DC and AC specifications. The Analog Devices AD6645-105 is a 14-bit, 105 MSPS converter featuring a 270-MHz input bandwidth, ± 0.5 least significant bit (LSB) of differential nonlinearity (DNL), ± 1.5 LSB of integral nonlinearity (INL), signal-to-noise ratio of 74.5 dB with 30.5-MHz input and spurious free dynamic range (SFDR) of 89 dBc ($70\text{MHz} < f_{\text{IN}} < 105\text{ MHz}$). The Texas Instruments ADS5500 is also a 14-bit converter with a maximum sampling rate of 125 MSPS with a 750-MHz analog bandwidth, ± 0.75 LSB DNL, ± 2.5 LSB INL, 71.5 dB SNR (30-MHz input), and 84-dBc SFDR (30-MHz input).

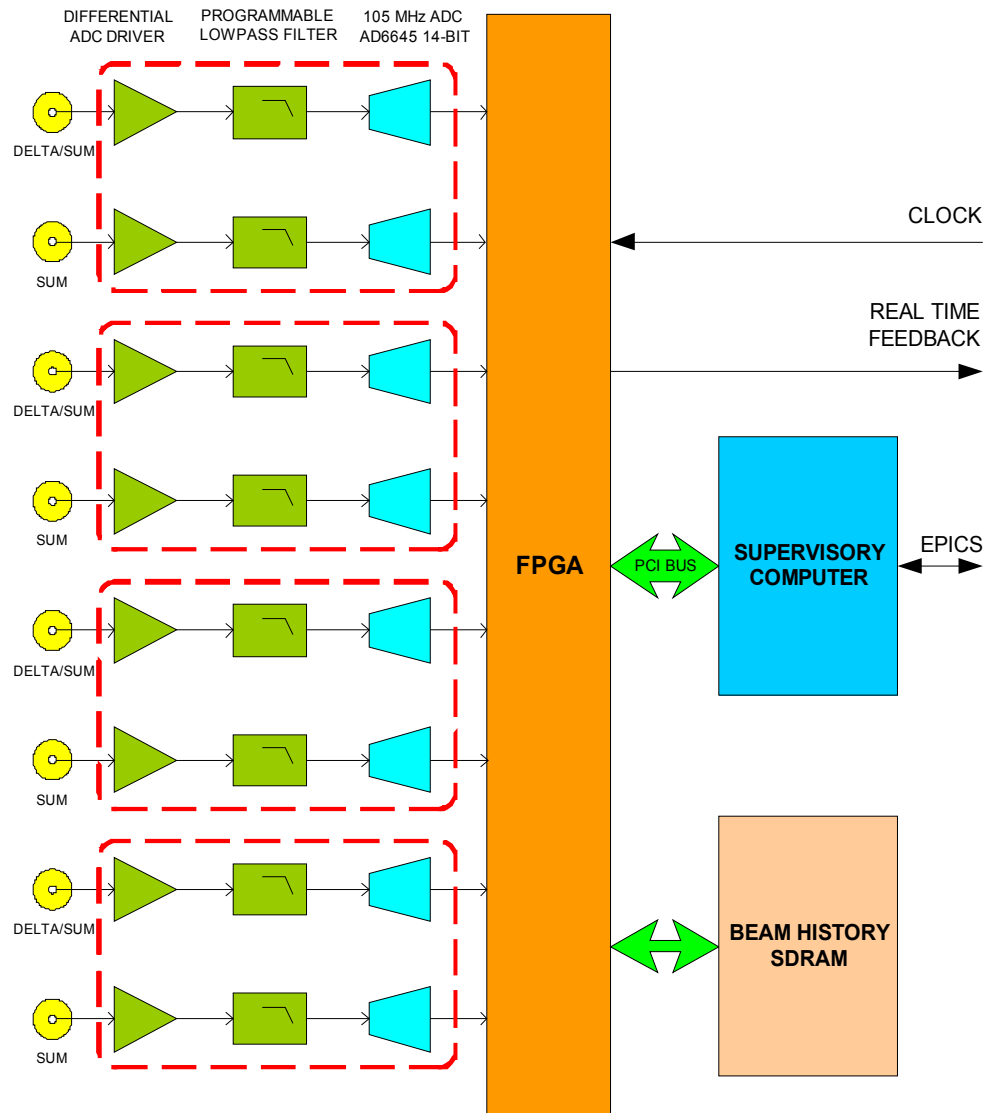


FIGURE 2. Data acquisition block diagram to process four BPMs.

Field Programmable Gate Array

Figure 3 illustrates a single channel for the Altera Stratix™ field-programmable gate array (FPGA). The clock generation and synchronization block accepts the 44-MHz clock and ‘PO’ marker from the facility timing system and uses these signals to synthesize an 88-MHz sampling clock to drive the analog-to-digital converters and a ‘beginning of turn’ marker to control the calculation of the turn-by-turn position information. This block also contains information about the fill pattern within the storage ring. This information is used to enable the summation block only when valid position signals are present. By performing the gated integration after digitization, the problems of drift and offset in the analog portion of the circuit are avoided.

The turn-by-turn beam position history is stored in a separate RAM module. A 128-Mbyte module will allow several seconds of turn-by-turn position information to be recorded.

The use of a single FPGA chip to perform the initial signal processing for all analog input channels has a number of advantages over a design using conventional digital-signal-processing devices. The FPGA chosen has several multiply/accumulate cores, which allows the signal processing for up to eight input channels to be performed on a single chip. This provides increased reliability and reduces power consumption since almost all high-speed signals are contained within that single device and need not pass through I/O pin drivers. Altera high-density Stratix™ FPGA devices have several features that make them attractive for this application.

1) Up to 22 high-performance DSP blocks per device; dedicated multiplier, pipeline, and accumulation circuitry. These blocks will be used to perform the initial gated averaging and statistics computation as well as the low-pass filtering of the turn-by-turn position information.

2) High-speed differential I/O interface support for connection to the high-speed serial interface, which will carry the filtered position information to the orbit correction computers.

3) Support for interfaces to high-speed external memory devices, including DDR and SDR SDRAM. External memory devices will be used to store the turn-by-turn beam history for post-fault analysis or diagnostic studies.

4) Full-featured phase lock loops (PLLs) for system timing management. The on-chip PLLs will be used to synchronize the data acquisition with the system 44-MHz and P0 clocks as well as obtaining time stamp and other information from the event system.

5) Up to 7 Mbits of embedded memory. This high-speed on-chip memory will be used for buffering sample-by-sample or bunch-by-bunch information for diagnostic studies.

6) Remote system update capability makes it easy to modify filter parameters and other system features without removing the board from the VXI crate and without transporting programming equipment to the rack in which the crate is installed.

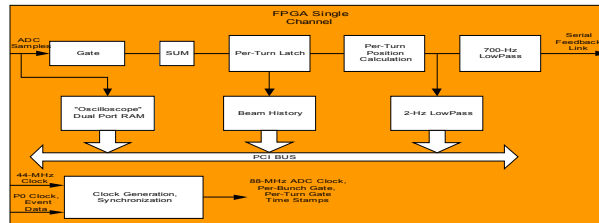


FIGURE 3. FPGA single-channel block diagram.

SPECIFICATION

The general system specifications are described below and in Table 1. The original specifications quoted in Table 1 are archived from the early commissioning days and are typically exceeded in routine operation at this time.

- 1) Measures beam position both during injection at 2 Hz and with stored beam.
- 2) Provides single-bunch tracking around the ring.
- 3) Measures position of different bunches at each BPM turn-to-turn.
- 4) Measures position at each turn (3.68 μ s revolution period).
- 5) Provides average beam position for higher accuracy.
- 6) Provides a 32,768 sample of the beam history for each BPM.

Parameter	Original Specification Limit	Specification Goal	Condition
First Turn, Single Bunch Resolution / Accuracy	< 200 μm / 500 μm rms	< 100 μm / 250 μm rms	Single Shot
Stored Beam, Single Bunch Resolution / Accuracy	< 25 μm / 200 μm rms	< 1 μm / 50 μm rms	0.1 Hz BW
Stored Beam, 24 Bunch or greater Resolution / Accuracy	< 25 μm / 200 μm rms	< 250 nm / 50 μm rms	0.1 Hz BW
Real Time Feedback, (24 Bunch or greater) Resolution	NEW	<500 nm rms	0.1-30 Hz BW
Real Time Feedback, (24 Bunch or greater) Resolution	NEW	< 2 μm rms	1-1000 Hz BW
Bunch-Bunch Oscilloscope mode (Stored Beam, Single or Multiple Bunches) Resolution / Accuracy	NEW	< 15 μm rms/ 50 μm rms	10 MHz BW
Dynamic Range, Position	\pm 20 mm Minimum	\pm 10 mm Minimum	Standard Chamber
Dynamic Range, Intensity Single Bunch 0.1-10 ma	\geq 40 dB	\geq 40 dB	200 μm deviation
Stability, Long Term	\pm 30 μm rms	\pm 1 μm rms	24 Hour +/- 0.2 Celsius

TABLE 1. General system specifications.

PERFORMANCE

Development on this project has just started and we are currently evaluating the Analog Device AD6645 ADC coupled to the high-speed ADC FIFO evaluation kit. The evaluation kit interfaces the ADC and provides a 256-k FIFO buffered memory, which captures the high-speed output of the AD6645. The kit also provides a software application to calculate real-time FFTs and time domain analysis. The monopulse receiver and the evaluation components were tested with 100 mA of stored beam with an equally spaced 24-bunch fill. The number of samples collected in the FIFO was varied and the noise floor relative to the ADC full-scale value was measured. A calculation based on the receiver + ADC measurement shown in Fig. 4 indicates an rms system noise floor of less than 10 nm / square root Hz can be realized. Further testing will continue after the May shutdown to fully quantify ADC dynamic performance and integrate FPGA processing.

DISCUSSION

The plan is to couple the ADC evaluation board to the FPGA development board to expedite the FPGA software development. The first task for the FPGA development will be to average 5-7 samples at the 88-MHz sample rate. In the next phase we are planning to build and test a single channel from ADC through to the FPGA interface. In parallel with the FPGA development we will continue system simulations to optimize filter requirements.

AD6645 Noise Floor Measurements

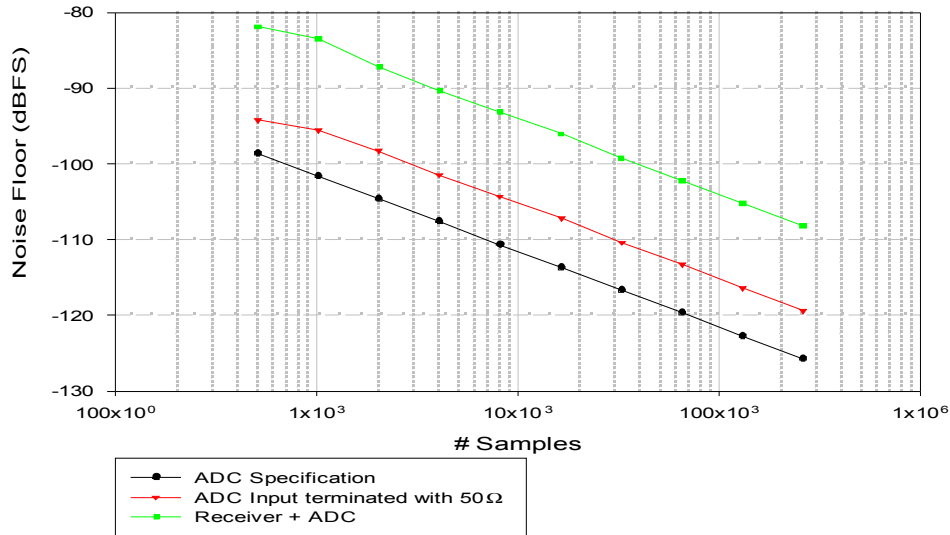


Figure 4. ADC noise floor.

ACKNOWLEDGMENTS

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